Amendments to the Specification:

Please amend the paragraph beginning on line 7 of page 6 as follows:

The compare enable bit 28 may indicate to the DMA controller 11 when to perform an operation (e.g., a comparison operation) based on the source address register 24 and the target address register 23. For example, when the compare enable bit is set to a first binary value (e.g., "0"), the DMA controller may not perform an operation (e.g., a comparison operation). For example, when the compare enable bit is set to a second binary value (e.g., "1"), the DMA controller 11 may perform an operation (e.g., a comparison operation). For example, the DMA controller 11 may compare the transfer data ~~indictor~~ indicator 18 identified by the address 31 in the source address register 24 with the data 30 of the target address register 23. If the identified transfer data indicator 18 matches the data 30 of the target address register 23, the DMA controller may set a compare status bit 34 (Figure 3) of the control status register 13 to a second binary value (e.g., "1"). A match may indicate that the target 15 is full.

Please amend the paragraph beginning on line 9 of page 10 as follows:

The descriptor 430 of the third type may be a descriptor to indicate that the data transfer must be stopped. The data transfer may be stopped because, for example, the target 15 is full or the end of a non-cyclic descriptor chain is reached. The descriptor 430 of the third type may include data for a command register 431, a target address register 432, a source address register 433, and a descriptor address register 434. For the command register 431, the transfer

length may be set to 0 bytes, the burst size may be set to 0 bytes, the compare enable bit may be set to a first binary value (e.g., "0") indicating the DMA controller may not perform a comparison operation, and the branch enable bit may be set to a first binary value (e.g., "0") indicating the DMA controller may not perform a branch operation. The target address register 432 may include a do not care entry for the address of the target 15. The source address register 433 may include a do not care entry for the address of the source 14. The descriptor address register 434 may include a do not care entry for the address of the memory 16 and may also include the stop bit set to a second binary value (e.g., "1"). The transfer length in the command register 431 being set to 0 bytes and the stop bit in the descriptor address register 434 being set to a second binary value (e.g., "1") may indicate that data transfer is to be stopped and that the DMA channel is to be deactivated.

Please amend the paragraph beginning on line 7 of page 12 as follows:

In the above exemplary embodiments, the compare enable bit 28 and the branch enable bit 29 may indicate when the DMA controller 11 is to perform a compare operation and a branch operation, respectively. In Figure 4, the compare enable bit 28 and the branch enable bit 29 may be enabled simultaneously (i.e., set to a second binary value (e.g., "1")). In another exemplary embodiment of the invention, the compare enable bit 28 and the branch enable bit 29 may be enabled in separate descriptors. For example, in descriptor N of the descriptor chain, the compare enable bit may be set to a second binary value (e.g., "1"), and the compare enable bit

may be set to a ~~second~~ first binary value (e.g., "0"). In descriptor N+M of the descriptor chain, the compare enable bit may be set to a first binary value (e.g., "0"), and the compare enable bit may be set to a second binary value (e.g., "1"). During data transfer, the DMA controller 11 may perform the comparison operation for descriptor N and the branch operation for descriptor N+M.